REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed May 5, 2004. Reconsideration and allowance of the application and pending claims are respectfully requested.

I. Allowable Subject Matter

Applicant appreciates the Examiner's indication that claims 1-12 are allowed and claims 16-18, and 21 would be allowable if rewritten to include all of the limitations of the base claim and any intervening claims.

In that it is believed that every rejection has been overcome, it is submitted that each of the claims that remains in the case is presently in condition for allowance.

II. Claim Objections

The Office Action notes the following claim objections:

> Claims 16-18, 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant believes that the rejection to claims 13 and 21 have been overcome through this response, and thus respectfully submit that the objection to the claims that depend therefrom have been overcome.

III. Claim Rejections - 35 U.S.C. § 103(a)

A. Rejection of Claims

Claims 13-15, 20, and 22 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Ravanelli, et al. ("*Ravanelli*", U.S. Pat. No. 5,789,785) in view of Colclaser, et al. ("*Colclaser*", U.S. Pat. No. 6,327,125). Applicant respectfully traverses this rejection.

B. The Colclaser and Ravanelli References

Colclaser discloses electrostatic discharge (ESD) disconnection techniques (col.3, lines 7-8), that make use of fuses in conjunction with ESD circuits. Whether placed in an I/O path, or across two rails, or both, the specification provides that "all ESD protection circuits are decoupled by opening the corresponding fuses (col. 4, lines 7-37). This decoupling of the ESD circuits during normal operation is further emphasized in col. 4, lines 38-40 of the specification:

> Generally, ESD protection circuits should appear as an open circuit in normal circuit function, and act as a discharge path only for ESD events.

With regard to capacitive loading and higher frequency operation, the specification provides the following (col. 5, lines 21-40):

> ESD protection techniques presently known to the inventors are suitable for circuits which operate in the 1-2 GHz range, but are expected to impose too high of a capacitive load for next-generation RF circuits for which operation above 10 GHz, and more particularly in the 30-40 GHz range is desired. Decoupling by active devices such as a pass gate will not be effective, as this type of device provides capacitance from gate to supply to ground, forming an unacceptable link for the signal. By contrast, disconnection of the ESD devices by a fuse element substantially eliminates capactive coupling of the ESD devices and the fuses

> themselves. Thus, when fuses are configured to be programmed via external connection pins of a completed (packaged) IC as in the present invention, the benefits of maintaining full ESD protection until the IC is placed in a system (as provided by a pass gate or other active circuit element in known devices) are retained, while the drawbacks of such active circuit elements (complexity, capacitive loading) are eliminated.

Thus, from the specification of *Colclaser*, it would appear that using active circuit elements are disfavored in light of the capacitive loading to the operational circuit. Further, it appears that it is intended that the ESD circuit in *Colclaser* be disconnected during normal operation, preferably through the use of fuses.

Ravanelli discloses an active device to provide ESD protection as shown in FIG. 2, yet as correctly noted in the Office Action, fails to "disclose that the protected circuit operates at a high frequency, above 1 GHz."

C. Discussion of the Rejection

As acknowledged by the Court of Appeals for the Federal Circuit, the U.S. Patent and Trademark Office ("USPTO") has the burden under section 103 to establish a proper case of obviousness by showing some objective teaching in the prior art or generally available knowledge of one of ordinary skill in the art that would lead that individual to the claimed invention. *See In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). Accordingly, to make a proper case for obviousness, there must be some prior art teaching or established knowledge that would suggest to a person having ordinary skill in the pertinent art to fill the voids apparent in the applied reference. It is respectfully asserted that no such case has been made in the outstanding Office Action.

In addition to the above-described defect of the rejection, Applicant respectfully asserts that the proposed combination is improper. It has been well established that teachings of references can be combined only if there is some suggestion or incentive to do so. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990). Accordingly, there must be a teaching in the relevant art which would suggest to a person having ordinary skill in that art the desirability of using an active device, such as a bipolar junction transistor as described in claims 13 and 20, at frequencies above approximately 1 GHz. In light of the cited sections of the specification noted in section (III)(B) above, and the fact that a prior art reference must be considered in its entirety, *i.e.*, as a whole, including portions that would lead away from the claimed invention (*W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983); and also see MPEP 2141.03), Applicant respectfully submits that no such motivation has been established. In fact combining the two references is actually contrary to what is being taught among the same.

The Office Action notes the following with regard to the combination of *Colclaser* and *Ravanelli*:

> Ravanelli et al disclose in Figure 2 an ESD protection circuit using a bipolar NPN transistor Q1 in reverse mode from a pad T1 to a ground T2 for biCMOS Ics. It does not disclose that the protected circuit operates at a high frequency, above 1GHz.
>
> Colclaser et al disclose that biCMOS Ics require ESD protection and that they operate currently in the 1-2 GHz range and next generation RF circuits are expected to operate above 10GHz, see 5:20-25. Also, the

> protection circuit can be implemented in any of the standard processes, such as bipolar, CMOS, or biCMOS; see 5:40-43.
>
> It would have been obvious to one having ordinary skill in the art at the time of the invention to have modified Ravanelli et al with the teachings of Colclaser et al and minimize capacitive loading on the protected circuit and extend performance at higher frequencies.

Applicant respectfully submits that there is no motivation to combine *Colclaser* and *Ravanelli*. Further bolstering this assertion is the fact that *Colclaser* teaches away from the active device approach of *Ravanelli*. As explained in section (III)(B) above, although *Colclaser* indicates that "ESD protection techniques presently known to the inventors are suitable for circuits which operate in the 1-2 GHz range," it does not indicate what types of ESD protection devices are used at those frequencies. The *Bertin* patent (USPN 5731945) is referenced as a prior art ESD protection device in *Colclaser*, but a search through that patent does not reveal any discussion on frequency of operation. Thus, the device in *Bertin* does not appear to be the ESD protection, suitable for higher frequencies, that *Colclaser* had in mind for higher frequencies. Further, there is no discussion in *Ravanelli* regarding high frequency operation or capacitive effects. Additionally, *Colclaser* teaches disconnecting the ESD circuits through fuses, unlike what is taught in *Ravanelli*.

Thus, assuming the hypothetical person skilled in the art who is interested in ESD protection at high frequency operation, such a person may consult the *Ravanelli* reference based on the ESD aspect. However, the design disclosed in *Ravanelli* would provide no indication of performance at high frequency. Assuming this hypothetical person skilled in the art consulted *Colclaser* for the high frequency aspect of ESD protection, it is likely he or she would likely be discouraged from using the active device approach of *Ravanelli*

to ESD protection in light of the teachings away from active devices due to capacitive effects as explained in section (III)(B) above, or perhaps equally as likely, would discount the use of *Colclaser* due to its teachings of the need for fuses (see col. 4, lines 14-16, for example). In either case, it is unlikely the hypothetical person skilled in the art would combine the teachings of *Colclaser* and *Ravanelli*.

Thus, Applicant respectfully submits that the combination of *Colclaser* and *Ravanelli* is improper, and thus a prima facia case of obviousness has not been established for the claim limitations "coupling said transistor between the circuit operating at a frequency above about 1 GHz and a pad coupled to the circuit," as recited in claim 13, nor for the claim limitation "operating the bipolar junction transistor in reverse mode between a transmission line and ground to protect the circuit operating at a frequency above approximately 1 GHz from electrostatic discharge," as recited in claim 20.

In summary, it is Applicant's position that a proper case for obviousness has not been made against Applicant's independent claim 13 and 20, and claims 14-18 and 21-22 (and newly added dependent claims 23-30) which respectively depend therefrom. Therefore, it is respectfully submitted that each of these claims is patentable over *Ravanelli* in view of *Colclaser*, and that the rejection of these claims should be withdrawn.

IV. Newly Added Claims

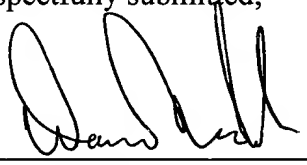
As identified above, claims 23-30 have been added into the application through this response. Applicant respectfully submits that these new claims, which depend from what Applicant respectfully submits is an allowable independent claim (independent claim 20),

describe an invention that is novel and unobvious in view of the prior art of record and, therefore, respectfully requests that these claims be held to be allowable.

CONCLUSION

Applicant respectfully submits that Applicant's pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

Respectfully submitted,



David Rodack
Registration No. 47,034

THOMAS, KAYDEN,
HORSTEMEYER & RISLEY, L.L.P.
Suite 1750
100 Galleria Parkway N.W.
Atlanta, Georgia 30339
(770) 933-9500

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Alexandria, Virginia 22313-1450, on 7-27-04.

Mary Meegan
Signature